APPENDIX

Changes to Specification:

Page 2, line 22, is deleted.

Page 2, after paragraph **[0005]**, a new heading is added.

The following are marked-up versions of the amended paragraphs:

Page 1, lines 1-4:

~~DESCRIPTION~~

PIEZOELECTRIC DEVICE AND METHOD FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

~~Technical Field~~1. Field of the Invention

Page 1, line 8:

~~Background Art~~2. Description of Related Art

[0008] One exemplary embodiment of the ~~The~~ present invention ~~in claim 1~~ is a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element both included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern on the base through a plurality of bumps.

[0009] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 2 is a~~ the piezoelectric device described above, ~~according to claim 1, wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals on the center portion of an active element surface of the semiconductor integrated circuit.

[0010] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 3 is~~ ~~a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are concentrically formed about the center of an active element surface of the semiconductor integrated circuit.

[0011] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 4 is~~ ~~a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

[0012] In another exemplary embodiment of the ~~The~~ present invention, in ~~claim 5 a~~ the piezoelectric device ~~according to claim 4~~ described above, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

[0013] In another exemplary embodiment of the ~~The~~ present invention, ~~in claim 6 is~~ ~~a~~ the piezoelectric device ~~according to claim 1,~~ described above further ~~comprising~~ includes a layered part, which surrounds the semiconductor integrated circuit, for mounting the piezoelectric resonator, the layered part ~~comprising~~ including at least two layers, including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

[0014] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 7 is~~ ~~a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

[0015] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 8 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ the base ~~comprises~~ may consist of a ceramic composite substrate.

[0016] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 9 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is an Au bump.

[0017] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 10 is a~~ the piezoelectric device ~~according to claim 1~~ described above, ~~wherein~~ a protrusion is formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

[0018] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 11 is a~~ the piezoelectric device ~~according to claim 10~~ described above, ~~wherein~~ the protrusion is formed in each of the side walls of the base facing the two sides along the longitudinal direction of the semiconductor integrated circuit.

[0019] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 12 is a~~ the piezoelectric device ~~according to claim 10~~ described above, ~~wherein~~ the protrusion formed in the side wall of the base has substantially the same height as, or is higher than, the semiconductor integrated circuit.

[0020] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 13 is a~~ the piezoelectric device ~~according to claim 10~~ described above, ~~wherein~~ a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit is set to a range between 0.05 and 0.15 mm.

[0021] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 14~~ is a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a

piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the opening, and the semiconductor integrated circuit is connected to the electrode pattern of the base through the plurality of bumps.

[0022] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 15 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are formed at regular intervals at the center portion of the active element surface of the semiconductor integrated circuit.

[0023] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 16 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ a dummy bump is formed on the active element surface of the semiconductor integrated circuit.

[0024] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 17 is a~~ the piezoelectric device ~~according to claim 16~~ described above, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit is connected to the electrode pattern on the base.

[0025] In another exemplary embodiment of the present ~~The~~ invention, ~~in claim 18 is a~~ the piezoelectric device ~~according to claim 14~~ described above, further includes ~~comprising~~ a layered part on which the piezoelectric resonator is mounted and which surrounds the semiconductor integrated circuit, the layered part ~~comprising~~ including at least two layers including a first layer and a second layer, wherein an opening of the first layer is formed to be larger than an opening of the second layer.

[0026] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 19 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

[0027] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 20 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ the base ~~comprises~~ includes a ceramic composite substrate.

[0028] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 21 is a~~ the piezoelectric device ~~according to claim 14~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

[0029] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 22~~ is a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, wherein an opening is formed in the center of a base provided with an input/output electrode pattern is formed, a plurality of bumps are formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit is mounted in the center of the opening, and the semiconductor integrated circuit is connected to the electrode pattern through the plurality of bumps by ultrasonic bonding ~~means~~.

[0030] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 23 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit is perpendicular

to the two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

[0031] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 24 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ a printing direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

[0032] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 25 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one having a diameter 0.8 to 0.9 times and the other having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

[0033] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 26 is a~~ the piezoelectric device ~~according to claim 25~~ described above, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit is shaped to have two levels, one being 80 to 90 μm in diameter and 30 to 35 μm in height, and the other being 40 to 45 μm in diameter and 30 to 35 μm in height.

[0034] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 27 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ the base ~~comprises~~ consists of a ceramic composite substrate.

[0035] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 28 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit are Au bumps.

[0036] In another exemplary embodiment of the present ~~The~~ invention, in ~~claim 29 is a~~ the piezoelectric device ~~according to claim 22~~ described above, ~~wherein~~ the longitudinal direction of the electrode pattern on the base and a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit are the same.

[0037] In another exemplary embodiment of the present ~~The~~ invention, ~~in claim 30 is a~~ the piezoelectric device ~~according to claim 22, comprising~~ described above includes the semiconductor integrated circuit and the piezoelectric resonator element in included in the package, wherein a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit and a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package are different from each other.

[0038] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 31~~ is a method for manufacturing a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method may include: ~~comprising:~~ a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which the metallic bump is formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

[0039] Another exemplary embodiment of the present ~~The~~ invention ~~in claim 32~~ is a method for manufacturing a piezoelectric device ~~comprising~~ including a semiconductor integrated circuit and a piezoelectric resonator element included in a package, the method ~~comprising~~ may include: a step of forming a metallic bump on the semiconductor integrated circuit; a step of connecting the semiconductor integrated circuit on which metallic bump is

formed to the base by ultrasonic bonding; a step of detecting a height direction of the semiconductor integrated circuit during the ultrasonic bonding step; a step of filling an underfill material around the semiconductor integrated circuit so as to cover the entire semiconductor integrated circuit including a rear surface of the semiconductor integrated circuit; a step of mounting the piezoelectric resonator element; and a step of hermetically sealing a metallic lid to the base.

Page 7, line 22:

~~Brief Description of the Drawings~~

BRIEF DESCRIPTION OF THE DRAWINGS

[0040] Figs. 1(A)-(B) are~~Fig. 1 is a~~ structural diagrams~~diagram~~ of a piezoelectric device according to the present invention;

Fig. 2 is a diagram illustrating the formation of a bump on a wafer of the piezoelectric device of the present invention;

Fig. 3 is a diagram showing the shape of the bump of the piezoelectric device of the present invention;

Fig. 4 is a diagram showing the shape of another bump of the piezoelectric device of the present invention;

Fig. 5 is a process diagram illustrating a flip-chip bonding process of the present invention;

Fig. 6 is a stress distribution map according to FEM analysis;

Fig. 7 is a structural diagram showing another embodiment of the present invention;

Fig. 8 is a structural diagram showing another embodiment of the present invention;

Fig. 9 is a structural diagram showing another embodiment of the present invention;

Figs. 10(A)-(B) are~~Fig. 10 is~~ a plan view and a front view, respectively, showing another embodiment of the present invention;

Figs. 11(A)-(B) are~~Fig. 11 is~~ a plan view and a front view, respectively, showing another embodiment of the present invention;

Fig. 12 is a structural diagram showing another embodiment of the present invention;

Fig. 13 is a structural diagram showing a cross-section of a bonded portion of the present invention;

Fig. 14 is a structural diagram showing yet another embodiment of the quartz crystal oscillator of the present invention;

Fig. 15 is an enlarged plan view showing a structure of a portion AR in Fig. 14; and

Figs. 16(A)-(B) are~~Fig. 16 is a~~ structural diagrams~~diagram~~ of a conventional piezoelectric device.

Page 8, line 25:

~~Best Mode for Carrying Out the Invention~~

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0043] ~~Fig. 1 is a~~ Figs. 1(A)-(B) are structural ~~diagram~~ diagrams of a surface-mount type quartz crystal oscillator according to an embodiment of the present invention.

[0044] As shown in a plan view of Fig. 1(A) and in a front view of Fig. 1(B), on a first layer of a base 1 ~~comprising~~ consisting of a ceramic insulating substrate having at least three layers and a seal ring of Fe-Ni alloy or the like, stamped to a frame shape, an electrode pattern 3 for forming a connection with a semiconductor integrated circuit (IC chip: hereinafter referred to as the IC chip) 2 is metallized by means of printing by using metal wiring material such as W (tungsten), Mo (molybdenum). On the top thereof, Ni plating and Au plating, etc., are provided.

[0058] The wafer IC chip 2 is picked up by a nozzle such as an inverted pyramidal ~~collet,~~ collet, is turned over, and is passed on to an nozzle tip of an ultrasonic horn. Then, the IC chip 2 is aligned and is chip-mounted on a mounting area of the base 1 with high precision by a system such as an image recognition system provided in the flip-chip bonding apparatus.

[0066] As shown in ~~Fig. 1,~~ Figs. 1(A)-(B), a configuration in which an opening 16 is formed in the center of the base 1 and the IC chip 2 is mounted in the center of the opening 16 is employed. Thus, when the quartz crystal oscillator 13 is exposed to stress, by this configuration, the stress is evenly applied to the IC chip 2, preventing the stress from concentrating in a specific portion.

[0077] As shown in ~~Fig. 1,~~ Figs. 1(A)-(B), the AT-cut quartz crystal resonator 6 is connected and fixed by the conductive adhesive 9 to mounting electrodes 21 and 22 of the mounting portion 8 provided in the second layer 5 of the base 1.

[0089] Furthermore, in order for the underfill material 23 to properly permeate to the bonded portion of the bumps 4, the second layer 5 on which the AT-cut quartz crystal resonator 6 is mounted ~~comprises~~ may include two layers, i.e., ~~an a~~ a first layer 24 ~~(first layer)~~ and a ~~b~~ second layer 25 ~~(second layer)~~. The opening portion of the ~~a~~ first layer 24 is formed to be larger than the opening portion of the ~~b~~ second layer 25. By forming the second layer ~~5~~ 25 in such a manner, the underfill material 23 properly permeates to the bonded portion of the bumps 4 and a highly reliable bonding structure is obtained.

[0107] In this embodiment, the vibration direction US2 of the ultrasonic waves for ultrasonic bonding and for forming bumps on the IC chip 2 shown in Fig. 15, and vibration direction US1 of the ultrasonic waves for performing a ultrasonic bonding of the IC chip 2 and the base 1 shown in Fig. 14 are set to be different, preferably, in directions which differ from one another by 90 degrees.

Changes to Claims:

The following are marked-up versions of the amended claims:

1. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit having a plurality of bumps formed thereon; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being ~~both~~ included in a package,

~~wherein an opening is formed in a center of a base provided with an input/output electrode pattern,~~ the semiconductor integrated circuit ~~is~~ being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit ~~is~~ being connected to an input/output electrode pattern on the base through ~~a~~ the plurality of bumps.

2. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being formed at regular intervals on a center portion of an active element surface of the semiconductor integrated circuit.

3. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being concentrically formed about a center of an active element surface of the semiconductor integrated circuit.

4. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ further comprising a dummy bump ~~is~~ formed on an active element surface of the semiconductor integrated circuit.

5. (Amended) The piezoelectric device according to claim 4, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit ~~is~~ being connected to the electrode pattern on the base.

7. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, a first level ~~one~~ having a diameter 0.8 to 0.9 times and ~~the other~~ a second level having a diameter 0.4 to 0.45 times a length of a side of an opening in a pad provided on an active element surface of the semiconductor integrated circuit.

8. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ the base ~~comprises~~ comprising a ceramic composite substrate.

9. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being an Au bump.

10. (Amended) The piezoelectric device according to claim 1, ~~wherein~~ a protrusion ~~is~~ being formed in at least one side wall of the base facing the side of the semiconductor integrated circuit.

11. (Amended) The piezoelectric device according to claim 10, ~~wherein~~ the protrusion ~~is~~ being formed in each of side walls of the base facing two sides along the longitudinal direction of the semiconductor integrated circuit.

12. (Amended) The piezoelectric device according to claim 10, ~~wherein~~ the protrusion formed in the side wall of the base ~~has~~ having a substantially same height as, or is higher than, the semiconductor integrated circuit.

13. (Amended) The piezoelectric device according to claim 10, wherein a gap between the protrusion formed in the side wall of the base and the semiconductor integrated circuit ~~is~~ being set to a range between 0.05 and 0.15 mm.

14. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

~~wherein an opening is formed in the center of a base provided with an input/output electrode pattern,~~ a plurality of bumps ~~are~~ being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit ~~is~~ being mounted in an opening formed in a center of a base, and the semiconductor integrated circuit ~~is~~ being connected to an input/output electrode pattern of the base through the plurality of bumps.

15. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being formed at regular intervals at a center portion of the active element surface of the semiconductor integrated circuit.

16. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ further comprising a dummy bump ~~is~~ formed on the active element surface of the semiconductor integrated circuit.

17. (Amended) The piezoelectric device according to claim 16, ~~wherein~~ the dummy bump formed on the semiconductor integrated circuit ~~is~~ being connected to the electrode pattern on the base.

19. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, ~~one~~ a first level having a diameter 0.8 to 0.9 times and ~~the other~~ a second level

having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

20. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ the base ~~comprises~~ comprising a ceramic composite substrate.

21. (Amended) The piezoelectric device according to claim 14, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being Au bumps.

22. (Amended) A piezoelectric device, comprising:

a semiconductor integrated circuit; and

a piezoelectric resonator element, the semiconductor integrated circuit and the piezoelectric resonator element being included in a package,

~~wherein an opening is formed in the center of a base provided with an input/output electrode pattern,~~ a plurality of bumps ~~are~~ being formed at two opposing sides of an active element surface of the semiconductor integrated circuit, the semiconductor integrated circuit ~~is~~ being mounted in a center of an opening formed in a center of a base, and the semiconductor integrated circuit ~~is~~ being connected to an input/output electrode pattern through the plurality of bumps by ultrasonic bonding ~~means~~.

23. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit ~~is~~ being perpendicular to two opposing sides of the active element surface of the semiconductor integrated circuit at which the plurality of bumps are formed.

24. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ a printing direction of the electrode pattern on the base ~~and~~ being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit ~~are the same~~.

25. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, ~~one~~ a first level having a diameter 0.8 to 0.9 times and ~~the other~~ a second level having a diameter 0.4 to 0.45 times the length of an opening in a pad provided on the active element surface of the semiconductor integrated circuit.

26. (Amended) The piezoelectric device according to claim 25, ~~wherein~~ each of the plurality of bumps formed on the semiconductor integrated circuit ~~is~~ being shaped to have two levels, ~~one~~ a first level being 80 to 90 μm in diameter and 30 to 35 μm in height, and ~~the other~~ a second level being 40 to 45 μm in diameter and 30 to 35 μm in height.

27. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ the base ~~comprises~~ comprising a ceramic composite substrate.

28. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ the plurality of bumps formed on the semiconductor integrated circuit ~~are~~ being Au bumps.

29. (Amended) The piezoelectric device according to claim 22, ~~wherein~~ a longitudinal direction of the electrode pattern on the base ~~and~~ being the same as a vibration direction of ultrasonic waves applied to the semiconductor integrated circuit ~~are the same~~.

30. (Amended) The piezoelectric device according to claim 22, ~~comprising the semiconductor integrated circuit and the piezoelectric resonator element in included in the package,~~

~~wherein~~ a vibration direction of ultrasonic waves for ultrasonic bonding and for forming bumps on the semiconductor integrated circuit ~~and~~ being different from a vibration direction of ultrasonic waves for performing ultrasonic bonding of the semiconductor integrated circuit to the package ~~are different from each other~~.